R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – I
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	Solid State Device Modeling and Simulation	MTVD-1001	3L-1T	4

Subject code:- MTVD-1001

Subject Name: - Solid State Device Modeling and Simulation

Course Outcomes

Students will

CO1 Learn Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources.

CO2 Get Knowledge of Injection and Transport Model, Continuity Equation, Diode Small Signal and Large Signal (Change Control Model), Transistor Models: Ebber - Molls and Gummel Port Model, Mextram model, SPICE modeling temperature and area effects.

CO3 Learn about MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

CO4 Learn about Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, etc.

CO5 Understand Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo-detectors.

SYLLABUS

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources.

Injection and Transport Model, Continuity Equation, Diode Small Signal and Large Signal (Change Control Model), Transistor Models: Ebber - Molls and Gummel Port Model, Mextram model, SPICE modeling temperature and area effects.

Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Biopolar and MOS Transistors.

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo-detectors.

REFERENCE BOOKS

1. Philip E. Allen, Douglas R. Hoberg, "CMOS Analog Circuit Design", Second Edition, Oxford Press, 2002.
2. S.M.Sze "Semiconductor Devices - Physics and Technology", John Wiley and sons, 1985
3. Kiat Seng Yeo, Samir S.Rofail, Wang-Ling Gob, "CMOS / BiCMOS ULSI - Low Voltage, Low
Power", Person education, Low price edition, 2003.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – I
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	CMOS Analog Circuit Design	MTVD-1002	3L-1T	4

Subject code:- MTVD-1002

Subject Name: - CMOS Analog Circuit Design

Course Outcomes:

The purpose of this course is to develop a strong base in design and analysis of CMOS analog circuits design and simulation using SPICE.

Students will

CO1 Learn about analog and digital signals, analog sampled-data or discrete time signal, circuit design, analysis of a circuit, synthesis of a circuit, differences between integrated and discrete analog circuit design, design process of an analog integrated circuit.

CO2 Get basic concepts of MOS fabrication processes, PN junction, MOS transistor, passive components, lateral and substrate BJT and latchup.

CO3 Get Knowledge of Large-signal and small-signal model for the MOS transistor, computer simulation models, simulation of MOS circuits using SPICE

CO4 Learn basics of MOS switch, MOS diode/ active resistor, current sinks and sources, current mirrors, current and voltage references, bandgap reference, simulation of CMOS sub circuits using SPICE.

CO5 Know about Common-Source stage (with resistive load, diode connected load, current-source load,triode load, source degeneration), source follower, common-gate stage, cascode stage, folded cascode stage, simulation of CMOS amplifiers using SPICE.

CO6 Attain Knowledge of Single-ended operation, differential operation, basic differential pair, large-signal and small-signal behavior, common-mode response, differential pair with MOS loads, simulation of differential amplifiers using SPICE.

CO7 Get the concept of op-amp, two-stage CMOS op-amp, cascode op-amps, 741 op-amp circuit, dc & small-signal analysis of 741 op-amp, simulation of 741 op-amp using SPICE, macro models for op-amps.Frequency response of CS stage, CD stage, CG stage, cascode stage, differential pair, two-stage CMOS opamp, folded cascode op-amp and 741 op-amp.

CO8 Learn about Noise characteristics in the frequency and time domains, thermal noise, shot noise, flicker noise, popcorn noise, noise models of IC components, representation of noise in circuits, noise in single-stage amplifiers (CS, CD and CG stages), noise in differential pairs, noise bandwidth, noise figure, noise temperature

SYLLABUS

CMOS Technology & Device Modeling

Introduction: Terminologies – analog and digital signals, analog sampled-data or discrete time signal, circuit design, analysis of a circuit, synthesis of a circuit, differences between integrated and discrete analog circuit design, design process of an analog integrated circuit.

CMOS Technology: Basic MOS fabrication processes, PN junction, MOS transistor, passive components, lateral and substrate BJT and latchup.

CMOS Device Modeling: Large-signal and small-signal model for the MOS transistor, computer simulation models, simulation of MOS circuits using SPICE.

CMOS subcircuits

MOS switch, MOS diode/ active resistor, current sinks and sources, current mirrors, current and voltage references, bandgap reference, simulation of CMOS sub circuits using SPICE.

CMOS amplifiers: Common-Source stage (with resistive load, diode connected load, current-source load, triode load, source degeneration), source follower, common-gate stage, cascode stage, folded cascode stage, simulation of CMOS amplifiers using SPICE.

Differential amplifier: Single-ended operation, differential operation, basic differential pair, large-signal and small-signal behaviour, common-mode response, differential pair with MOS loads, simulation of differential amplifiers using SPICE.

Operational Amplifiers & Frequency Response

Performance parameters of op-amp, two-stage CMOS op-amp, cascode op-amps, 741 op-amp circuit, dc & small-signal analysis of 741 op-amp, simulation of 741 op-amp using SPICE, macro models for op-amps. Frequency response of CS stage, CD stage, CG stage, cascode stage, differential pair, two-stage CMOS opamp, folded cascode op-amp and 741 op-amp.

Noise Characteristics

Noise characteristics in the frequency and time domains, thermal noise, shot noise, flicker noise, popcorn noise, noise models of IC components, representation of noise in circuits, noise in single-stage amplifiers (CS, CD and CG stages), noise in differential pairs, noise bandwidth, noise figure, noise temperature.

REFERENCE BOOKS

1. Allen, Holberg, “CMOS analog circuit design”, Oxford University Press, 2004.
2. Razavi, “Design of analog CMOS integrated circuits”, McGraw Hill, 2001.
3. Gray, Meyer, Lewis, Hurst, “Analysis and design of Analog Integrated Circuits”, 4th Edition, Willey International, 2002.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – I
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	Digital Signal Processing Structures for VLSI	MTVD-1003	3L-1T	4

Subject code:- MTVD-1003

Subject Name: - Digital Signal Processing Structures for VLSI

Course Outcomes:

DSPs are used in many application areas and hence have become an essential part of VLSI. This course is intended to introduce the students about DSP structures, this subject is included. After this course the student will know fundamentals of DSP and various structures useful in DSP implementation

Students will learn

CO1 **Introduction to Digital Signal Processing**
Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters - Filter Realizations. Representation of DSP Algorithms - Block diagram-SFG-DFG.

CO2 **Iteration Bound, Pipelining and Parallel Processing of FIR Filter**
Iteration Bound: Data-Flow Graph Representations- Loop Bound and Iteration Bound- Algorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters- Parallel Processing- Pipelining and Parallel Processing for Low Power.

CO3 **Fast Convolution and Arithmetic Strength Reduction in Filters**
Fast Convolution: Cook-Toom Algorithm- Modified Cook-Toom Algorithm.Design of Fast Convolution, Algorithm by Inspection. Parallel FIR filters-Fast FIR algorithms-Two

parallel and three parallel. Parallel architectures for Rank Order filters-Odd Even Merge sort architecture-Rank Order filter architecture-Parallel Rank Order filters-Running Order Merge Order Sorter-Low power Rank Order filter.

CO4 **Pipelined and Parallel Recursive Filters**

Pipelined and Parallel Recursive Filters : Pipeline Interleaving in Digital Filters-Pipelining in 1st Order IIR, Digital Filters- Pipelining in Higher- Order IIR Filters-Clustered Look ahead and Stable Clustered Look ahead- Parallel Processing for IIR Filters and Problems.

CO5 **Scaling and Round off Noise**

Scaling and Round off Noise: Scaling and Round off Noise- State Variable Description of Digital Filters, Scaling and Round off Noise Computation.

SYLLABUS

Introduction to Digital Signal Processing

Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters -Filter Realizations. Representation of DSP Algorithms - Block diagram-SFG-DFG.

Iteration Bound, Pipelining and Parallel Processing of FIR Filter

Iteration Bound: Data-Flow Graph Representations- Loop Bound and Iteration Bound-Algorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters- Parallel Processing- Pipelining and Parallel Processing for Low Power. Retiming: Definitions- Properties and problems- Solving Systems of Inequalities.

Fast Convolution and Arithmetic Strength Reduction in Filters

Fast Convolution: Cook-Toom Algorithm- Modified Cook-Toom Algorithm.Design of Fast Convolution Algorithm by Inspection. Parallel FIR filters-Fast FIR algorithms-Two parallel and three parallel. Parallel architectures for Rank Order filters-Odd Even Merge sort architecture-Rank Order filter architecture-Parallel Rank Order filters-Running Order Merge Order Sorter-Low power Rank Order filter.

Pipelined and Parallel Recursive Filters

Pipelined and Parallel Recursive Filters : Pipeline Interleaving in Digital Filters- Pipelining in 1st Order IIR Digital Filters- Pipelining in Higher- Order IIR Filters-Clustered Look ahead and Stable Clustered Look ahead- Parallel Processing for IIR Filters and Problems.

Scaling and Roundoff Noise

Scaling and Roundoff Noise : Scaling and Roundoff Noise- State Variable Description of Digital Filters- Scaling and Roundoff Noise Computation-Round Off Noise Computation Using State Variable Description- Slow-Down- Retiming and Pipelining.

REFERENCE BOOKS

1. K.K Parhi, "VLSI Digital Signal processing", John-Wiley, 1999.

2. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1995.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – I
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	Low Power VLSI Design	MTVD-1004	3L-1T	4

Subject code:- MTVD-1004

Subject Name: - Low Power VLSI Design

Course Outcomes

CO1 **Introduction to low power VLSI design and analysis**
Introduction to low power VLSI design-Need for low power-CMOS leakage current-static current-Basic principles of low power design-probabilistic power analysis-random logic signal-probability and frequency power analysis techniques-signal entropy.

CO2 **Circuit level and logic level design techniques**
Circuit - transistor and gate sizing - pin ordering - network restructuring and reorganization – adjustable threshold voltages - logic-signal gating - logic encoding. Pre-computation logic.

CO3 **Special low power VLSI design techniques – I**
Power reduction in clock networks - CMOS floating node - low power bus - delay balancing - SRAM.

CO4 **Special low power VLSI design techniques – II**
Switching activity reduction - parallel voltage reduction - operator reduction -Adiabatic computation – pass transistor logic

CO5 **Software design and power estimation**
Low power circuit design style - Software power estimation – co-design.

SYLLABUS

1. Introduction to low power VLSI design and analysis

Introduction to low power VLSI design-Need for low power-CMOS leakage current-static current-Basic principles of low power design-probabilistic power analysis-random logic signal-probability and frequency power analysis techniques-signal entropy.

2. Circuit level and logic level design techniques

Circuit - transistor and gate sizing - pin ordering - network restructuring and reorganization – adjustable threshold voltages - logic-signal gating - logic encoding. Pre-computation logic.

3. Special low power VLSI design techniques – I

Power reduction in clock networks - CMOS floating node - low power bus - delay balancing - SRAM.

4. Special low power VLSI design techniques – II

Switching activity reduction - parallel voltage reduction - operator reduction -Adiabatic computation – pass transistor logic

5. Software design and power estimation

Low power circuit design style - Software power estimation – co-design.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – I

Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	Graph Theory and Optimization Techniques	MTVD-1005	3L-1T	4

Subject code: - MTVD-1005

Subject Name: - Graph Theory and Optimization Techniques

Course Outcomes:

This Course is aimed at providing graph theory and optimization techniques for use in VLSI design. At the end of this course the student will be able to know, graph theory basics, application of it in optimization techniques. Students will learn

CO1 **Paths and Circuits**
Graphs – Data structures for graphs – Subgraphs – Operations on Graphs Connectivity – Networks and the maximum flow – Minimum cut theorem – Trees – Spanning trees – Rooted trees – Matrix representation of graphs.

CO2 **Graphs & Graph Colorings**
Eulerian graphs and Hamiltonian graphs – Standard theorems – Planar graphs – Euler's formula Five colour theorem – Coloring of graphs – Chromatic number (vertex and edge) properties and examples – Directed graphs

CO3 **Applications**
Computer Representation of graphs – Basic graph algorithms – Minimal spanning tree

algorithm – Kruskal and Prim's algorithm – Shortest path algorithms – Dijsktra's algorithm – DFS and BFS algorithms.

CO4 **Optimization Techniques**
Single variable and multivariable optimization – Lagrangian method – Kuhn-Tucker conditions – Random pattern and Random search methods

CO5 **Unconstrained Minimization Methods**
Classification – Techniques of unconstrained minimization – Scaling of Design variables – Direct search methods – Random jumping method – Grid search method – Univariate method – Hook and Jeeve's method – Newton – Raphson method – Fibonacci method.

SYLLABUS
Paths and Circuits

Graphs – Data structures for graphs – Subgraphs – Operations on Graphs Connectivity – Networks and the maximum flow – Minimum cut theorem – Trees – Spanning trees – Rooted trees – Matrix representation of graphs.

Graphs & Graph Colorings

Eulerian graphs and Hamiltonian graphs – Standard theorems – Planar graphs – Euler's formula Five colour theorem – Coloring of graphs – Chromatic number (vertex and edge) properties and examples – Directed graphs

Applications
Computer Representation of graphs – Basic graph algorithms – Minimal spanning tree algorithm – Kruskal and Prim's algorithm – Shortest path algorithms – Dijsktra's algorithm – DFS and BFS algorithms.

Optimization Techniques

Single variable and multivariable optimization – Lagrangian method – Kuhn-Tucker conditions – Random pattern and Random search methods.

Unconstrained Minimization Methods

Classification – Techniques of unconstrained minimization – Scaling of Design variables – Direct search methods – Random jumping method – Grid search method – Univariate method – Hook and Jeeve's method – Newton – Raphson method – Fibonacci method.

REFERENCE BOOKS
1. Narsingh Deo, "Graph Theory with Applications to Engineering and Computer Science," PHI.
2. Rao S.S., "Engineering Optimizations: Theory and Practice", New Age International Pvt. Ltd., 3rd
Edition, 1998.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – II
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	Testing of VLSI Circuits	MTVD-2001	3L-1T	4

Subject code: - MTVD-2001

Subject Name: - Testing of VLSI Circuits

Course Outcomes:

Testing VLSI is essential as these circuits are complex. Hence this course deals with fundamental techniques used for logic testing. At the end of the course the student will be having knowledge on digital testing as applied to VLSI design. Students will get the knowledge of

CO1 **Basics of Testing and Fault modeling**
Introduction - Need for testing - VLSI Testing Process And Test Equipment - Types of testing - ATE ADVANTEST model T6682-Block Diagram and Specification– Electrical Parametric testing – AC and DC Test Economics - Fault Molding-Stuck at faults. Calculation of DCR and ECR.

CO2 **Test generation for combinational circuits**

Faults in Digital circuits-failures and faults. Modeling of faults. Temporary faults. Test generation for combinational logic circuits-combinational ATPG-Boolean Difference Method-D-Algorithm-PODEM-FAN. Algorithm. Testable combinational logic circuit design. Algorithm for true value simulation and for fault simulation.

CO3 **Test generation and Testability of sequential circuits**

Test generation for sequential circuits. Design of testable sequential circuits-sequential ATPG Implementation and complexity- Time Frame Expansion-simulation method. DSP based testing - Static ADC & DAC testing methods- Testable memory design –Reduced Functional Faults-MARCH and MAT+ algorithm. Analog and Mixed signal tests.

CO4 **Memory, Delay fault and IDDQ Testing**

Delay test - Path delay test and fault models - Transition faults - delay test methodologies – practical consideration - IDDQ testing - Testing methods - Limitations of IDDQ testing - DFT IDDQ.

CO5 **Built-in Self-Test.**

DFT - Scan Design - Partial scan design - BIST- TPG for BIST - output response analysis, BIST Architectures- Random Logic BIST - Memory and delay fault BIST - JTAG - System test and core based design.

Digital VLSI Design- MTVD-202

Course Outcomes:

This course deals with fundamentals of electronics involved in the design of VLSI circuits. At the end of the course, students will understand CMOS processing technology and Basic CMOS circuits, characteristics and performance, designing of combinational and sequential circuits in CMOS. Students will learn about

CO1 **Introduction to MOS Device**

MOS Transistor-First Glance at the MOS device MOS Transistor under static conditions-threshold voltage, Resistive operation-saturation region -channel length modulation-velocity saturation-Hot carrier effect-drain current Vs voltage charts - sub threshold conduction - equivalent resistance-MOS structure capacitance, Design logic gates using NMOS and PMOS and CMOS devices-Stick Diagram.

CO2 **MOS Transistor Device Modeling**

Modeling of MOS Transistor using modeling technique-various model CMOS Inverter. Performance of propagation delay sizing inverter consumption-static consumption PSPICE-Introduction – Basic Concepts-LEVEL1-LEVEL2-LEVEL3 comparison. Static CMOS inverter, Evaluating the Robustness of CMOS inverter: Dynamic Behavior-computing the capacitance-for performance-sizing a chain of invertors - Dynamic power

CO3 **CMOS combinational logic design**

Static CMOS design-complementary CMOS - static properties- complementary CMOS design-Power consumption in CMOS logic gates-dynamic or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic - Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection -Designing logic for reduced supply voltages.

CO4 **CMOS sequential logic design**

Timing metrics for sequential circuit -latches Vs registers -static latches and registers - Bistability principle multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non, Bistable sequential circuit-Schmitt trigger-mono stable –Astable -sequential circuit - choosing a clocking strategy.

CO5 **CMOS subsystem design**

Data Path Operations: Addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- ALUs Multiplication- Shifters- Memory elements- control: Finite-State Machines.

SYLLABUS

Basics of Testing and Fault modeling

Introduction - Need for testing - VLSI Testing Process And Test Equipment - Types of testing - ATE ADVANTEST model T6682-Block Diagram and Specification– Electrical Parametric testing – AC and DC Test Economics - Fault Molding-Stuck at faults. Calculation of DCR and ECR.

Test generation for combinational circuits

Faults in Digital circuits-failures and faults. Modeling of faults. Temporary faults. Test generation for combinational logic circuits-combinational ATPG-Boolean Difference Method-D-Algorithm-PODEM-FAN. Algorithm. Testable combinational logic circuit design. Algorithm for true value simulation and for fault simulation.

Test generation and Testability of sequential circuits

Test generation for sequential circuits. Design of testable sequential circuits-sequential ATPG Implementation and complexity- Time Frame Expansion-simulation method. DSP based testing - Static ADC & DAC testing methods- Testable memory design –Reduced Functional Faults-MARCH and MAT+ algorithm. Analog and Mixed signal tests.

Memory, Delay fault and IDDQ Testing

Delay test - Path delay test and fault models - Transition faults - delay test methodologies – practical consideration - IDDQ testing - Testing methods - Limitations of IDDQ testing - DFT IDDQ.

Built-in Self-Test.

DFT - Scan Design - Partial scan design - BIST- TPG for BIST - output response analysis, BIST

Architectures- Random Logic BIST - Memory and delay fault BIST - JTAG - System test and core based design.

REFERENCE BOOKS

1. Parag.K.Lala "Digital Circuit Testing and Testability" Academic Press.
Viswani D. Agarval Michael L. Bushnell, "Essentials of Electronic Testing for Digital Memory &

Mixed Signal VLSI Circuit", Kluwer Academic Publications, 1999

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – II

Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	Digital VLSI Design	MTVD-2002	3L-1T	4

Subject code:- MTVD-2002

Subject Name: - Digital VLSI Design

Course Outcomes:

This course deals with fundamentals of electronics involved in the design of VLSI circuits. At the end of the course, students will understand CMOS processing technology and Basic CMOS circuits, characteristics and performance, designing of combinational and sequential circuits in CMOS. Students will learn about

CO1 **Introduction to MOS Device**

MOS Transistor-First Glance at the MOS device MOS Transistor under static conditions-threshold voltage, Resistive operation-saturation region -channel length modulation-velocity saturation-Hot carrier effect-drain current Vs voltage charts - sub threshold

conduction - equivalent resistance-MOS structure capacitance, Design logic gates using NMOS and PMOS and CMOS devices-Stick Diagram.

CO2 **MOS Transistor Device Modeling**

Modeling of MOS Transistor using modeling technique-various model CMOS Inverter. Performance of propagation delay sizing inverter consumption-static consumption PSPICE-Introduction – Basic Concepts-LEVEL1-LEVEL2-LEVEL3 comparison. Static CMOS inverter, Evaluating the Robustness of CMOS inverter: Dynamic Behavior-computing the capacitance-for performance-sizing a chain of invertors - Dynamic power

CO3 **CMOS combinational logic design**

Static CMOS design-complementary CMOS - static properties- complementary CMOS design-Power consumption in CMOS logic gates-dynamic or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic - Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection -Designing logic for reduced supply voltages.

CO4 **CMOS sequential logic design**

Timing metrics for sequential circuit -latches Vs registers -static latches and registers - Bistability principle multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non, Bistable sequential circuit-Schmitt trigger-mono stable –Astable -sequential circuit - choosing a clocking strategy.

CO5 **CMOS subsystem design**

Data Path Operations: Addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- ALUs Multiplication- Shifters- Memory elements- control: Finite-State Machines.

SYLLABUS

Introduction to MOS Device

MOS Transistor-First Glance at the MOS device MOS Transistor under static conditions-threshold voltage, Resistive operation-saturation region -channel length modulation-velocity saturation-Hot carrier effect-drain current Vs voltage charts - sub threshold conduction - equivalent resistance-MOS structure capacitance, Design logic gates using NMOS and PMOS and CMOS devices-Stick Diagram.

MOS Transistor Device Modeling

Modeling of MOS Transistor using modeling technique-various model CMOS Inverter. Performance of propagation delay sizing inverter consumption-static consumption PSPICE-Introduction – Basic Concepts-LEVEL1-LEVEL2-LEVEL3 comparison. Static CMOS inverter, Evaluating the Robustness of CMOS inverter: Dynamic Behavior-computing the

capacitance-for performance-sizing a chain of invertors - Dynamic power

CMOS combinational logic design

Static CMOS design-complementary CMOS - static properties- complementary CMOS design-Power consumption in CMOS logic gates-dynamic or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic - Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection - Designing logic for reduced supply voltages.

CMOS sequential logic design

Timing metrics for sequential circuit -latches Vs registers -static latches and registers - Bistability principle multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non, Bistable sequential circuit-Schmitt trigger-mono stable –Astable -sequential circuit - choosing a clocking strategy.

CMOS subsystem design

Data Path Operations: Addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- ALUs Multiplication- Shifters- Memory elements- control: Finite-State Machines.

REFERENCE BOOKS

1. Jan.M.Rabaey., Anitha Chandrakasan Borivoje Nikolic, "Digital Integrated Circuits", Second Edition.

2. Neil H.E Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Addition Wesley, 1998.

3. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital IC- Analysis and Design”, 3rd Edition, Tata McGraw Hill publication.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – II
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	DSP Architectures and Applications	MTVD-2003	3L-1T	4

Subject code: - MTVD-2003

Subject Name: - DSP Architectures and Applications

Course Outcomes:

This course introduces Digital Signal processors. At the end of this course the student will know various DSPs and their architectures and uses. Students will get the knowledge of

CO1 **Overview of Digital Signal Processing**

Advantages of DSP over analog systems, salient features and characteristics of DSP systems, applications of DSP systems, Introduction to DSP Processors: Common features of DSP processors, numeric representations in DSP processor, data path of a DSP processor, memory structures in DSP processors, VLIW architecture, special addressing modes in DSP processors, pipelining concepts, on-chip peripherals found in DSP

processors.

CO2 **TMS320C5X Processors**

Architecture of TMS320C5X Processors- Assembly Instructions- Addressing Modes- Pipelining and Peripherals- lab exercise.

CO3 **TMS320C3X Processors**

Architecture of TMS320C3X- Instruction Set- Addressing Modes- Data Formats- Floating Point Operation, Pipelining and Peripherals- lab exercise.

CO4 **Black fin Processor**

Introduction to Black fin processor- Architecture overview-processor core-addressing modes-instruction sets, Targeted applications- lab exercise.

CO5 **SHARC Processor**

VLIW Architecture- SHARC- SIMD- MIMD Architectures- Application: Adaptive filters-DSP based biometry receiver-speech processing-position control system for hard disk drive-DSP based power meter.

SYLLABUS

Overview of Digital Signal Processing

Advantages of DSP over analog systems, salient features and characteristics of DSP systems, applications of DSP systems, Introduction to DSP Processors: Common features of DSP processors, numeric representations in DSP processor, data path of a DSP processor, memory structures in DSP processors, VLIW architecture, special addressing modes in DSP processors, pipelining concepts, on-chip peripherals found in DSP processors.

TMS320C5X Processors

Architecture of TMS320C5X Processors- Assembly Instructions- Addressing Modes- Pipelining and Peripherals- lab exercise.

TMS320C3X Processors

Architecture of TMS320C3X- Instruction Set- Addressing Modes- Data Formats- Floating Point Operation, Pipelining and Peripherals- lab exercise.

Black fin Processor

Introduction to Black fin processor- Architecture overview-processor core-addressing modes-instruction sets, Targeted applications- lab exercise.

SHARC Processor

VLIW Architecture- SHARC- SIMD- MIMD Architectures- Application: Adaptive filters-DSP based biometry receiver-speech processing-position control system for hard disk drive-DSP based power meter.

REFERENCE BOOKS

1. B.Venkatramani & M.Baskar, "Digital Signal Processor", McGraw Hill, 2000
2. Avatar Singh and S. Srinivasan, “Digital signal processing”, Thomson books, 2004

3. K.K Parhi, “VLSI DSP Systems”, John Wiley, 1999.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – II
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	System on Chip Design	MTVD-2004	3L-1T	4

Subject code: - MTVD-2004

Subject Name: - System on Chip Design

Course Outcomes:

IP cores and application specific design is becoming the order of the day. Because of the usefulness of this for both VLSI and embedded students this subject is provided. To make the student learn System-on-chip fundamentals, their applications and On-chip networking methods. Student will get knowledge of

System on Chip Design - MTVD-2004

Course Outcomes:

IP cores and application specific design is becoming the order of the day. Because of the usefulness of this for both VLSI and embedded students this subject is provided. To make the student learn System-on-chip fundamentals, their applications and On-chip networking methods. Student will get knowledge of

CO1 **SOC fundamentals**
Essential issues of SoC design – A SoC for Digital still camera – multimedia IP development : Image and video codecs.

CO2 **SOC software and energy management**
SoC embedded software – energy management techniques for SoC design.

CO3 **On-chip networking System design and methodology**
Design methodology for NOC based systems – Mapping concurrent application onto architectural platforms.

CO4 **Hardware and basic infrastructure**
Packet switched network for on-chip communication – energy reliability tradeoff for NoC's – clocking strategies – parallel computer as a NoC's region.

CO5 **Software and application interfaces**
MP-SoC from software to hardware – NoC APIs – multilevel software validation for NoC – Software for network on chip

SYLLABUS

Part-A: SOC

SOC fundamentals

Essential issues of SoC design – A SoC for Digital still camera – multimedia IP development : Image and video codecs.

SOC software and energy management

SoC embedded software – energy management techniques for SoC design.

Part- B: On-chip networking

On-chip networking System design and methodology

Design methodology for NOC based systems – Mapping concurrent application onto architectural platforms.

Hardware and basic infrastructure

Packet switched network for on-chip communication – energy reliability tradeoff for NoC's – clocking strategies – parallel computer as a NoC's region.

Software and application interfaces
MP-SoC from software to hardware – NoC APIs – multilevel software validation for NoC – Software for network on chip

REFERENCE BOOKS
1. Axel Jantsch, Hannu Tenhunen, "Network on chips", Kluwer Academic Publishers, 2003.
2. Youn-Long, Steve Lin, "Essential Issues of SoC Design: Designing Complex Systems-On-Chip",
Springer, 2006.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
FIRST YEAR

Semester – II
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	Fundamentals and Application of Mems	MTVD-2005	3L-1T	4

Subject code: - MTVD-2005

Subject Name: - Fundamentals and Application of Mems

Course Outcomes:

This course is an introduction to MEMS, which also uses micro electronics. This course fulfills the need of electronic engineer who want to create MEMS devices. At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

CO1 **Overview of MEMS and Microsystems**
MEMS and Microsystems, Microsystems and microelectronics, Microsystems and miniaturization, Working principle of micro system – Micro sensors, Micro actuators, MEMS with Micro actuators.

CO2 **Materials For MEMS**
Substrate and Wafer, Silicon as a Substrate Material, Silicon Compound, Silicon Piezo-Resistors, Gallium Arsenide, Quartz, Piezoelectric Crystals, Polymers and Packaging Materials.

CO3 **Microsystems Fabrication Process**
Fabrication Process – Photolithography, Ion implantation, Oxidation, Chemical vapor deposition (CVD), Physical vapor deposition, Deposition by Epitaxy, Etching. Manufacturing Process – Bulk Micromachining, Surface Micromachining, LIGA Process.

CO4 **Microsystems Design, Assembly and Packaging**
Micro system Design – Design consideration, process design, Mechanical design, Mechanical design using MEMS, Mechanical packaging of Microsystems, Microsystems packaging, interfacing in Microsystems packaging, packaging technology, selection of packaging materials, signal mapping and transduction.

CO5 **Case Study of MEMS Devices**
Case study on strain sensors, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes , RF MEMS Switch, phase shifter, and smart sensors. Case study of MEMS pressure sensor Packaging.

SYLABUS

Overview of MEMS and Microsystems

MEMS and Microsystems, Microsystems and microelectronics, Microsystems and miniaturization, Working principle of micro system – Micro sensors, Micro actuators, MEMS with Micro actuators.

Materials For MEMS

Substrate and Wafer, Silicon as a Substrate Material, Silicon Compound, Silicon Piezo-Resistors, Gallium Arsenide, Quartz, Piezoelectric Crystals, Polymers and Packaging Materials.

Microsystems Fabrication Process

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(CVD), Physical vapor deposition, Deposition by Epitaxy, Etching. Manufacturing Process – Bulk Micromachining, Surface Micromachining, LIGA Process.

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Case Study of MEMS Devices

Case study on strain sensors, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes , RF MEMS Switch, phase shifter, and smart sensors. Case study of MEMS pressure sensor Packaging.

REFERENCE BOOKS

1. Tai – Rai Hsu, "MEMS and Microsystems DESIGN and Manufacturing", Tata MC Graw Hill, Edtion 2002.
2. Julian W Gardner, "Microsensors MEMS and smart devices", John Wiley and sons Ltd, 2001.
3. Chang Liu, "Foundation of MEMS", Pearson International Edition, 2006.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
SECOND YEAR

Semester – III

Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	ASIC Design	MTVD-3001(A)	3L-1T	4

Subject code: - MTVD-3001(A)

Subject Name: - ASIC Design

Course Outcomes:

As VLSI implementation is largely in ASIC, this course introduces the fundamentals of ASIC and its design methods. Students will learn

CO1 Types of ASICs – Design flow – CMOS transistors CMOS Design rules – Combinational Logic Cell Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance Logical effort – Library cell design – Library architecture.

CO2 Anti fuse – static RAM – EPROM and EEPROM technology – PREP benchmarks – Actel ACT – Xilinx, LCA – Altera FLEX – Altera Max DC & AC inputs and outputs – Clock & Power inputs – Xilinx I/O blocks.

CO3 Actel ACT –Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – Altera FLEX- Design systems – Logic Synthesis – Half gate ASIC –Schematic entry – Low level design language – PLA tools – EDIF- CFI design representation.

CO4 ASIC Construction: Physical Design- System Partitioning- FPGA Partitioning- Partitioning Methods. Floor planning and Placement: Floor planning- Placement- Physical Design Flow. Routing: Global Routing –Detailed Routing- special Routing. Design checks

CO5 Planar subset problem(PSP) –single layer global routing single layer detailed routing wire length and bend minimization technique-over the cell(OTC) Routing-multichip modules(MCM)-Programmable logic arrays, Transistor chaining-Weinberger Arrays-Gate Matrix Layout-ID Compaction-2D compaction

SYLLABUS

Types of ASICs – Design flow – CMOS transistors CMOS Design rules – Combinational Logic Cell Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance Logical effort – Library cell design – Library architecture.

Anti fuse – static RAM – EPROM and EEPROM technology – PREP benchmarks – Actel ACT – Xilinx, LCA – Altera FLEX – Altera Max DC & AC inputs and outputs – Clock & Power inputs – Xilinx I/O blocks.

Actel ACT –Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 –

Altera FLEX- Design systems – Logic Synthesis – Half gate ASIC –Schematic entry – Low level design language – PLA tools – EDIF- CFI design representation.

ASIC Construction: Physical Design- System Partitioning- FPGA Partitioning- Partitioning Methods. Floor planning and Placement: Floor planning- Placement- Physical Design Flow. Routing: Global Routing –Detailed Routing- special Routing. Design checks

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REFERENCE BOOKS

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison – Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice
Hall PTR, 2003.

R.K.D.F. UNIVERSITY, BHOPAL

M.TECH (VLSI)

SECOND YEAR

Semester – III

Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits

VLSI	Programming in HDL	MTVD-3002(A)	3L-1T	4

Subject code: - MTVD-3002(A)

Subject Name: - Programming in HDL

Course Outcomes:

HDL programming is fundamental for VLSI design and hence this course will helps the student to write programs in VHDL and Verilog HDL for modeling digital electronic circuits. The student will understand and learn

CO1 **Basic concepts:** Operators, Data types, Number specification, System tasks and compiler directives, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling-example for each modeling –test bench- lab exercise.

CO2 **Tasks and Functions-**example-useful modeling techniques-Timing and delays-Switch level modeling-user defined primitives- lab exercise.

CO3 **Basic Concepts**: Data Objects, Data Types, Operators, Concurrent and Sequential Assignment Statements, Different Styles of Modeling, Simple Examples-test bench- lab exercise.

CO4 **Procedure and functions -** examples-packages - Generic constants and statements - examples. Component and configuration- lab exercise.

CO5 **Introduction to synthesis** - Verilog synthesis-modeling tips for Verilog logic synthesis-combinational and sequential logic synthesis using VHDL-VHDL modeling restrictions-lab exercise.

SYLLABUS

Basic concepts: Operators, Data types, Number specification, System tasks and compiler directives, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling-example for each modeling –test bench- lab exercise.

Tasks and Functions-example-useful modeling techniques-Timing and delays-Switch level modeling-user defined primitives- lab exercise.

Basic Concepts: Data Objects, Data Types, Operators, Concurrent and Sequential Assignment Statements, Different Styles of Modeling, Simple Examples-test bench- lab exercise.

Procedure and functions - examples-packages - Generic constants and statements - examples. Component and configuration- lab exercise.

Introduction to synthesis - Verilog synthesis-modeling tips for Verilog logic synthesis-combinational and sequential logic synthesis using VHDL-VHDL modeling restrictions- lab exercise.

REFERENCE BOOKS

1. Samir Palnitkar,"Verilog HDL", Pearson education, 2004.
2. Peter J.Ashenden, "The designer guide to VHDL", 2001

M.TECH (VLSI)
SECOND YEAR

Semester – III
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credits
VLSI	Embedded Wireless Sensor Networks	MTVD-3002(B)	3L-1T	4

Subject code: - MTVD-3002(B)

Subject Name: - Embedded Wireless Sensor Networks

Course Outcomes:

This course will impart the fundamentals and the theory behind the wireless sensor networks and its applications. Students will learn about

CO1 **Introduction**
Embedded network systems – representation of signals – signal propagation – sensor principles.

CO2 **Communication**
Source detection and identification – digital communications – multiple source estimation and multiple access communications.

CO3 **Networking**
Networking – network position and synchronization services.

CO4 **Network management**
Energy management – data management – articulation mobility and infrastructure.

CO5 **Nodes, data and application**
Node architecture – network data integrity – experimental system design.

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SYLLABUS

Introduction
Embedded network systems – representation of signals – signal propagation – sensor principles.

Communication
Source detection and identification – digital communications – multiple source estimation and multiple access communications.

Networking
Networking – network position and synchronization services.

Network management
Energy management – data management – articulation mobility and infrastructure.

Nodes, data and application
Node architecture – network data integrity – experimental system design.

REFERENCE BOOKS
1. Gregory Pottie and William Waiger, “Principles of embedded networked system design”, Cambridge University Press, 2005.
2. Jr.Edger H. Callaway, “Wireless sensor networks”, CRC Press, 2004.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
SECOND YEAR

Semester – III
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credit
VLSI	Dissertation Part- I (Literature Review/Problem Formulation/ Synopsis	MTVD-3003	0L-0T-2P	2

Course Outcomes: After studying this course, students will be able to,

CO1- To define and limit of the research.

CO2- To place your study in an historical perspective.

CO3- To avoid unnecessary duplication.

CO4- To evaluate promising research methods.

Course Content

The objective of Dissertation Part-I is to promote a systematic understanding of the knowledge, critical awareness of current problems, originality in the application of knowledge and the quality of work. The ideal work may be characterized by a new result in design, development and implementation. It should have the potential of industrial/scientific acceptance. The first part of the Dissertation should be to determine the interest of students and broadly identify the area of work, finalize the research problem based on literature survey. Also, by now the students should have familiarity with the concepts, tools, techniques required to carry out the Dissertation work. Student is expected to start the research work. Outcome of Dissertation Part-I should be to conclude the work on the identified problem its importance, its justification, literature survey, field work, research work etc. Minor variation may be accepted depending upon nature of title.

R.K.D.F. UNIVERSITY, BHOPAL
M.TECH (VLSI)
SECOND YEAR

Semester – IV
Course Content & Grade

Branch	Subject Title	Subject Code	Contact Hours per Week	Total Credit
VLSI	Dissertation Part- II	MTVD-4001	0L-0T-2P	2

Course Outcomes: After studying this course, students will be able to,

CO1- The programme of instruction will consist of advanced subjects of the respective specialization. The complete programme is distributed over four semesters with two semesters per academic year. Course work is offered in the first two semesters (except for PG programme in Mechanical engineering where it is extended up to third semester) and the dissertation work will be carried out during third and fourth semesters. Every branch of M.E/ M. Tech programme will have a curriculum and syllabi for the courses recommended by the board of studies and approved by the academic council. The academic programmes of the Institute follow the credit system.

CO2- Every candidate shall be required to submit the record of dissertation work at the end of fourth semester.

Course Content

The objective of Dissertation Part-I is to promote a systematic understanding of the knowledge, critical awareness of current problems, originality in the application of knowledge and the quality of work. The ideal work may be characterized by a new result in design, development and implementation. It should have the potential of industrial/scientific acceptance. Dissertation Part-II should be seen in continuation with Dissertation Part-I. The researcher should continue the research work in the two parts.